

SEMICONDUCTOR SUBSTRATE, SOI SUBSTRATE AND  
MANUFACTURING METHOD THEREFOR

FIELD OF THE INVENTION AND RELATED ART:

5           The present invention relates to a substrate  
for a semiconductor apparatus, such as a SOI substrate  
or FET having a MFS structure (metal-film /  
ferroelectric-material-film / semiconductor layer  
structure), in which a crystalline insulation layer is  
10 provided on a silicon substrate with an insulation  
layer exhibiting an electrical insulation property or  
a micro machining property interposed therebetween  
such that semiconductor crystal layer or a  
ferroelectric crystal layer can be grown, and a  
15 manufacturing method therefor. The substrate for the  
semiconductor device in this invention includes a  
substrate which can be a complete base for a  
semiconductor device and a base on which crystalline  
semiconductor layer and a dielectric layer, the  
20 substrate partly having an insulative silicon compound  
layer or a crystalline insulation layer as will be  
described hereinafter, a substrate to be provided on a  
laminated semiconductor layer, and a substrate for  
micro machining having a crystalline insulation layer  
25 with an insulation layer to improve a micro machining  
property. Particularly, the substrate for the micro  
machine is used when machining is effected on top or

bottom of the substrate to permit repetitive fine mechanical deformation or vibration. An example of the substrate for micro machining comprises a silicon vibrational plate and a monocrystal PZT film formed thereon, wherein a liquid chamber is formed by etching  
5 a bottom side (unimorph structure), or a cantilever structure for reflecting light.

As for a SOI substrate with which a semiconductor crystal layer is formed on an insulation layer, for example, there are known a method in which  
10 two silicon substrates 2 having oxide films formed thereon are pasted to each other, and one of the substrates are removed by abrasion or etching so that thin semiconductor layer remains, or oxygen or the  
15 like is injected to a predetermined depth by ion injection from the surface of the silicon substrate, and then an annealing process is carried out, so that insulation layer is implanted into the semiconductor substrate. On the other hand, in a semiconductor  
20 memory device using a ferroelectric material layer, a ferroelectric material layer is laminated on a semiconductor layer, with or without an insulation film therebetween, or on a surface of an electrode metal such as platinum or the like. In the case of a  
25 MFS structure in which a ferroelectric material layer is laminated on a semiconductor layer, an oxide film is produced between the ferroelectric material layer

and the semiconductor layer with the result of deterioration of the crystallinity or morphology and increase of interface level density between the ferroelectric material layer and the semiconductor layer. Even if a ferroelectric material layer is laminated on an insulation film, it is not possible to grow a ferroelectric material layer having a sufficient crystallinity on an amorphous insulation film. With a method in which metal is oxidized, and simultaneously the silicon is also oxidized, a high quality insulation layer is not provided, and in addition, the crystal insulation layer thereon does not exhibit a sufficient orientation. In a manufacturing process for a semiconductor device, there is a case in which epitaxial growth of a semiconductor layer, a crystalline dielectric layer or the like is required on a semiconductor substrate with an insulation layer therebetween, but it is not possible to directly laminate a layer having a high crystallinity on the surface of an insulation layer. Recently, however, using said pasting method, a SOI method has been put into practice in which one of the silicon layer is thinned by abrasion, etching or water knife, but with this method, a very expensive process is required, so that substrate per se is expensive. For a structure for micro machine or the like, an inexpensive substrate and manufacturing method

therefor are desired. In a method in which oxygen or the like is implanted in the surface layer portion of the semiconductor substrate, the deterioration of the surface of the semiconductor layer by the ion  
5 implanting is significant, and the ion injection is again expensive, and therefore, the same problems are involved. As for a method in which epitaxial growth of YSZ thin film is effected on a silicon substrate, there is method disclosed in SHINGAKU GIHOU (ED96-42,  
10 CPM96-27, May, 1996) or a method disclosed in Japanese Laid-open Patent Application Hei 07-150361. According to these methods, an insulation layer having a crystalline property can be provided on a silicon substrate, and a semiconductor layer or ferroelectric  
15 material layer can be formed on the surface through epitaxial growth. However, the YSZ thin film formed on the silicon substrate is a crystalline metal oxide involving ion movement, and therefore, electrical insulation and the etching stop property when used for  
20 micro machining, are poorer than the silicon oxide film or the silicon nitride film, with the result of slight deterioration of the performance. Japanese Laid-open Patent Application Hei 10-265948 discloses that amorphous silicon oxide film is formed on  
25 crystalline silicon, and a crystalline insulation layer is further formed. This method is equivalent to a technique of forming an amorphous silicon oxide

layer and a crystalline insulation layer within oxygen  
ambience as disclosed in No.167 KENKYUKAISHIRYO (42-  
43) in a 131st thin film Committee of Japan GAKUJUTU  
SINKOUKAI held in HAKUUNRO HOTEL, May 31 - June 1,  
5 1993, and these methods involve a problem that  
resultant amorphous layer contains a large amount of  
impurity element because of introduction of oxygen  
during sputtering operation. Although the  
crystallinity of the produced crystalline insulation  
10 layer exhibits YSZ (111) matchable with silicon  
lattice matching, the orientation in the plane is not  
possible, so that no complete epitaxial layer can not  
be provided.

15 SUMMARY OF THE INVENTION:

These and other objects, features and  
advantages of the present invention will become more  
apparent upon a consideration of the following  
description of the preferred embodiments of the  
20 present invention taken in conjunction with the  
accompanying drawings.

Accordingly, it is a principal object of the  
present invention to provide a substrate for a  
semiconductor device, SOI substrate and a  
25 manufacturing method capable of manufacturing suchh  
substrates with low cost, which is suitable for growth  
of a crystal layer such as a semiconductor layer, a

ferroelectric material layer or the like on another semiconductor layer with an insulation layer therebetween in a semiconductor device manufacturing step, and an electrical insulation property relative  
5 to the silicon substrate which is the base, an etching stop property, or a repetitive vibration property for a micro actuator or the like, can be improved, with low cost.

According to an aspect of the present  
10 invention, there is provided a substrate for a semiconductor device comprising a crystalline silicon substrate; an insulative silicon compound layer thereon and a crystalline insulation layer on said insulative silicon compound layer, wherein said  
15 insulative silicon compound layer contains not more than 10at% of component element of a material constituting said crystalline insulation layer, the component element being provided in said insulative silicon compound layer by diffusion.

20 According to another aspect of the present invention, there is provided a SOI substrate comprising said substrate for the semiconductor device as defined in the above paragraph, further comprising a crystalline silicon on said crystalline insulation  
25 layer.

According to a further aspect of the present invention, there is provided a manufacturing method

for a semiconductor device substrate, comprising  
ejecting in non-active gas a metal oxide constituting  
a crystalline insulation layer; forming a crystal  
layer of a crystalline insulative material on a  
5 silicon substrate heated up to not lower than 400°C;  
forming an insulative silicon compound layer on said  
silicon substrate by oxygen diffusion from an oxide  
during said crystal layer formation step, oxygen  
diffusion during a temperature holding time after said  
10 crystal layer formation step and/or oxygen diffusion  
during cooling operation.

According to a further aspect of the present  
invention, there is provided a method for  
manufacturing SOI substrate comprising a method' as  
15 defined in the above paragraph, wherein crystalline  
silicon film is formed on the crystalline insulation  
layer which is formed on the silicon substrate.

According to the present invention, a  
structure is provided in which a crystalline  
20 insulation layer is formed on a silicon crystal layer  
with an amorphous insulation film of silicon compound  
exhibiting good insulation property and etching  
property, and therefore, another semiconductor layer  
or crystalline dielectric layer can be formed thereon  
25 by epitaxial growth, and a three-dimensional  
semiconductor device, a complex semiconductor device,  
a high performance semiconductor memory device can be

formed. A new highly integrated semiconductor devices  
can be manufactured with low cost. In addition, an  
oxide layer exhibiting a good etching property can be  
provided, and therefore, by combination with a highly  
5 oriented PZT, a micro actuator having a good vibration  
property can be formed. A new micro device can be  
manufactured with low cost.

These and other objects, features and  
advantageous of the present invention will become more  
10 apparent upon a consideration of the following  
description of the preferred embodiments of the  
present invention taken in conjunction with the  
accompanying drawings.

15 BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 illustrates a structure of a  
semiconductor device substrate according to an  
embodiment of the present invention.

Figure 2 is a schematic illustration of an  
20 example of a sputtering apparatus for epitaxial growth  
usable with a manufacturing method for the  
semiconductor device substrate according to the  
embodiment of the present invention.

Figure 3 is a schematic illustration of  
25 introduction, after completion of film formation by  
the sputtering apparatus of Figure 2, of oxygen with  
the temperature during the film formation; in (a) dry

O<sub>2</sub> is supplied; and in (b) water vapor O<sub>2</sub> is supplied.

Figure 4 is a schematic view illustrating an annealing process in the manufacturing method for the semiconductor device substrate according to the embodiment of the present invention; in (a) Ar+dry O<sub>2</sub> is supplied; in (b) Ar+water vapor O<sub>2</sub> is supplied.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS:

The preferred embodiments of the present invention will be described in conjunction with the accompanying drawings.

As shown in Figure 1, the substrate for the semiconductor device comprises a (crystalline) silicon substrate 1, a crystalline insulation layer 3 such as YSZ or the like, and an insulative silicon compound layer 2 such as silicon oxide film or the like which exhibits a high electrical insulation property and etching stop property.

The silicon substrate 1 comprises a silicon monocrystal layer of n-type, p-type or a type in which n-type region or p-type region is formed, and a semiconductor circuit is formed, or a type in which a silicon semiconductor layer is formed on another semiconductor layer or the like through epitaxial growth at its entire or partial surface.

The crystalline insulation layer (monocrystal insulation layer) 3 may be, for example, a metal oxide

with which a crystalline structure can be formed, and  
it may be YSZ (yttria-stabilized zirconia),  $\text{Al}_2\text{O}_3$   
(sapphire),  $\text{CeO}_2$  (ceria),  $\text{MgO}$  (magnesia),  $\text{SrTiO}_3$   
(strontium titanate),  $\text{ZrO}_2$  (zirconia) or the like with  
5 which a crystalline structure of a metal compound can  
be provided in the non-active gas. The thickness  
thereof, although it is different depending on the  
usage, is normally 5-20nm for a background for the  
growth of another semiconductor layer or crystalline  
10 dielectric layer, and it may be approx. 0.5-3 $\mu\text{m}$   
depending on the usage.

The insulative silicon oxide 2 may be a  
silicon oxide such as  $\text{SiO}_2$ , a silicon nitride such as  
 $\text{Si}_3\text{N}_4$ , silicon oxide nitride such as  $\text{SiON}$ . In the  
15 case of these compounds, with growth of the  
crystalline insulation layer 3, reaction occurs  
between the silicon in the substrate and the oxygen  
and/or nitrogen penetrating the crystalline insulation  
layer 3, and is limited to a compound of a material  
20 penetrating the crystalline insulation layer 3.  
During formation of the insulative silicon compound  
layer 2, element component constituting the  
crystalline insulation layer 3 is diffused and  
introduced. As readers the impurity element which is  
25 diffused and introduced, the inventors have revealed  
that insulation property and the etching property  
changes in accordance with the concentration of the

impurity element. As will be described hereinafter which Table 3, when the impurity element concentration (not less than 0at%) is not more than 10at%, the insulation property is high; and when it is not more  
5 than 7at%, particularly not more than 5at%, the etching property is high. On the basis of these findings, the concentration of the component element of material which constitutes the crystalline insulation layer 3 and which is diffused and  
10 introduced into the insulative silicon compound layer 2 is controlled to be not more than 10at%, preferably not more than 5at%. The thickness of the insulative silicon compound layer 2 is determined in consideration of the insulation property, etching stop  
15 property, micro machining property or the like, depending on the usage. Normally, it is 10-60nm.

According to the semiconductor device substrate of this embodiment, the monocrystal insulation layer 3 is provided on the silicon  
20 substrate 1 with the amorphous insulation film 2 therebetween, and therefore, the substrate has excellent electrical insulation property, etching stop property and micro machining property. In addition, the surface has a crystalline structure, and  
25 therefore, a semiconductor layer or a monocrystal dielectric layer can be formed on its surface through epitaxial growth. Since there is an amorphous

insulation film 2 of silicon compound between the silicon crystal layer 1 and the monocrystal insulation layer 3, the insulation property is excellent, and therefore, the electrical insulation is very high

5 between the layer formed on the surface of the crystalline insulation layer 3 and the silicon substrate 1 therebelow. The monocrystal insulation layer 3, as described herein before, is a metal compound, and therefore, ions are movable, and the

10 insulation property is slightly poor, but the silicon oxide or silicon nitride (silicon compound) exhibits excellent electrical property. When the crystalline insulation layer is produced by reaction with metal using reactive gas, a large amount of impurity element

15 is refused to the  $\text{SiO}_2$  layer interface which is an insulative silicon compound layer, and therefore, sufficient insulation property or etching stop property is not provided. However, according to an embodiment of the present invention using a non-active

20 gas such as Ar or the like, which will be described hereinafter, the impurity diffusion adjacent the interface can be suppressed to not more than 10at%. By limiting the impurity element concentration (not less than 0at%) to not more than 10at%, the insulation

25 property is excellent, and in addition by limiting it to not more than 7at%, particularly, not more than 5at%, the etching property is excellent.

As a result, as shown in Figure 1, a SOI substrate 6 can be provided by forming a film of crystalline silicon 4 on the crystalline insulation layer 3 in the semiconductor device substrate 5, or a YSZ layer may be further formed on the SOI substrate to provide a substrate in which the crystal silicon layer is sandwiched by insulative oxide layers. In addition, on a silicon crystal layer having a semiconductor circuit pattern thereon, a semiconductor layer is further formed with an insulation layer therebetween to form a three dimensional circuit. A crystalline dielectric layer of ferroelectric material can be formed with a clean crystalline structure to provide a high performance semiconductor memory device. A Si monocrystal portion of the above-described sandwich structure may be used as a vibrational plate, an electrode and PZT or PMN is formed on the insulative crystal YSZ through the epitaxial growth, which can be used as a micro actuator.

Referring to Figures 2 through 4, the description will be made as to a manufacturing method for a semiconductor device substrate according to an embodiment of the present invention, with which a crystal of crystalline insulation layer (YSZ) is grown on a silicon substrate with a silicon oxide film therebetween. Figure 2 schematically shows an example

of a sputtering apparatus for epitaxial growth, which is usable for manufacturing the substrate for the semiconductor device according to the embodiment of the present invention. Figure 3 is a schematic illustration of introduction, after completion of film formation by the sputtering apparatus of Figure 2, of oxygen with the temperature during the film formation; in (a) dry  $O_2$  is supplied; and in (b) water vapor  $O_2$  is supplied. Figure 4 is a schematic view illustrating an annealing process in the manufacturing method for the semiconductor device substrate according to the embodiment of the present invention; in (a) Ar+dry  $O_2$  is supplied; in (b) Ar+water vapor  $O_2$  is supplied.

In the sputtering apparatus 10 shown in Figure 2, the YSZ crystal is grown on the silicon substrate with the silicon oxide film therebetween. At this time, a substrate 11 of silicon semiconductor crystal layer having a diameter of 2in. Is mounted on a substrate mount 14 in the vacuum chamber 13, and a target 12 is fixed on a target holding Table 16 so as to be opposed to the substrate mount 14. The target 12 used was  $ZrO_2$  multiple oxide target comprising 5% of  $Y_2O_3$ . A frame 17 of permalloy encloses the target 12. The target supporting Table 16 is connected with a high oscillation voltage source through a matching circuit 19 to produce high frequency plasma discharge

in the vacuum chamber 13. Designated by 19a is a matching box.

One side wall of the vacuum chamber 13 is provided with an introduction tube 20 for introduction  
5 of the gas, through which non-active gas (Ar) is supplied into the vacuum chamber 13. The other side wall of the vacuum chamber 13 is provided with a gas discharge opening 21. A heater 15 is used to control heating and cooling of the substrate 11. The  
10 substrate 11 heated by the heater 15 is located right above the target 12 with a gap of 3cm. With the state, the sputtering film formation is carried out. As regards the temperature of the heater 15 hearing the film forming operation, the substrate temperature  
15 is not lower than 400°C, more particularly 600°C or 800°C for example.

Using such a sputtering apparatus 10, the non-active gas (Ar) is introduced into the vacuum chamber 13 through the introduction tube 20, the  
20 substrate is heated by the heater 15 to a temperature of not lower than 400°C, for example 600°C or 800°C, and the high oscillation voltage source is actuated to cause Ar discharge. The YSZ film formation conditions are as follows:

25           Input power: 200W (fixed)  
            Ar gas flow rate: 20sccm (fixed) and  
            Film formation time: 5 min.

With these conditions, metal (Zr, Y) is from the  $\text{ZrO}_2$  multiple oxide target 12 comprising  $\text{Y}_2\text{O}_3$  5%, and a crystal layer of crystalline insulative material (YSZ) of metal oxide of them can be formed on the  
5 silicon substrate 11.

After the thin layer is formed of metal Zr by the sputtering apparatus, a similar film formation may be effected by an oxide target.

After the completion of the film formation,  
10 oxygen (dry  $\text{O}_2$  or water vapor  $\text{O}_2$ ) is introduced through the introduction tube 20 such that internal pressure of the vacuum chamber 13 becomes 1atm while maintaining the temperature during the film formation for a predetermined duration by the heater 15. After  
15 elapse of predetermined maintaining duration, the heater 15 is deactuated, quick cooling is carried out with Ar replacement to increase the oxide film layer ( $\text{SiO}_2$ ) as the insulative silicon compound layer. This is shown in (a) and (b) of Figure 3. In (a) of Figure  
20 3, the dry  $\text{O}_2$  is supplied through a dryer 25 and a filter 26, and in (b) of Figure 3, water vapor  $\text{O}_2$  is provided by adding water vapor generated by heating water by water vapor to the  $\text{O}_2$  supplied through the dryer 25 and the filter 26. Table 1 shows a relation  
25 between a thickness of the oxide film layer and a temperature holding time under the constant temperature heating condition ( $600^\circ\text{C}$  and  $800^\circ\text{C}$  which

is the film formation temperature) after the completion of the heating film formation. In the case that quick cooling was effected with the Ar replacement without keeping the temperature after the completion of the film formation, the increase of the oxide film layer ( $\text{SiO}_2$ ) was not observed. From Table 1, it is understood that thickness of the oxide layer ( $\text{SiO}_2$ ) increases when the holding time is long and the atmosphere is water vapor  $\text{O}_2$ .

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Table 1

Thickness [nm] of oxide layer under 600 °C  
of film formation temperature

5	holding time	1min.	10min.	100min.	500min.
	dry O <sub>2</sub>	1	5	12.5	50
	water vapor O <sub>2</sub>	2.5	10	100	400
10					

Thickness [nm] of oxide layer under 800 °C  
of film formation temperature

15	holding time	1min.	10min.	100min.	500min.
	dry O <sub>2</sub>	2	10	25	100
	water vapor O <sub>2</sub>	5	20	200	800
20					

After the quick cooling of the silicon substrate together with Ar replacement, an annealing process is carried out using an electric furnace shown in Figure 4. In Figure 4, designated by 30 is an electric furnace including a heater 32 on its wall, and 33 is a substrate mount for mounting the substrate

31, which contains a heater therein. Designated by 34  
is a gas introduction opening for permitting  
introduction of gas into the electric furnace 30. The  
gas introduction opening 34 is provided with a dryer  
5 35 and a filter 36 ((a) of Figure 4) which are  
connected in series. There is further provided water  
vapor generating means 37 for generating water vapor  
by heating pure water ((b) of Figure 4).

Using such an apparatus, the annealing  
10 process is effected to the substrate for a  
predetermined time while keeping the temperature at  
not less than 600°C (annealing temperature). In the  
annealing process, the temperature has been set at  
600°C, 800°C and 1000°C, and the investigations has  
15 been made as to the relation among the thickness of  
the oxide film layer, the annealing temperature and  
the process time under the atmosphere of dry O<sub>2</sub> and  
water vapor O<sub>2</sub>. The results are shown in Table 2. As  
will be understood from Table 2, the oxide layer can  
20 be formed irrespective of the film thickness of the  
YSZ, and the annealing process can increase the oxide  
layer when the annealing temperature is high, and the  
atmosphere is the oxygen including the water vapor.

Table 2

Thickness [nm] of oxide layer under 600 °C  
of annealing

5 holding time 1min. 10min. 100min. 500min.

dry O<sub>2</sub> 1 5 12.5 50

water vapor O<sub>2</sub> 2.5 10 100 400

10

Thickness [nm] of oxide layer under 800 °C  
of annealing

15 holding time 1min. 10min. 100min. 500min.

dry O<sub>2</sub> 2 10 25 100

water vapor O<sub>2</sub> 5 20 200 800

20

25

Thickness [nm] of oxide layer under 1000 °C  
of annealing

holding time	1min.	10min.	100min.	500min.
dry O <sub>2</sub>	4	20	50	200
water vapor O <sub>2</sub>	10	40	400	1600

10

As described in the foregoing, the substrate is heated to not less than 400°C; the metal oxide constituting the crystalline insulation layer is ejected in the non-active gas atmosphere (Ar or the like) from the target to grow the crystal layer of the crystalline insulative material on the silicon substrate; and then an amorphous insulative silicon compound layer (SiO<sub>2</sub> or the like, which will simply be called "oxide layer") is formed by oxygen diffusion which is considered as being at least one of (1) the oxygen diffusion from the oxide during the film formation, (2) oxygen diffusion during the temperature holding time after the completion of the film formation, and (3) oxygen diffusion due to the oxygen during the cooling; and the component element of the material constituting the crystalline insulative material is introduced into the insulative silicon

25

compound layer by the diffusion. The distribution of the component element is such that it is large adjacent the interface between the crystalline insulative material layer and the insulative silicon compound layer, and gradually decreases away from the crystalline insulative material layer. Thus, the component element of the material constituting the crystalline insulative material is introduced and mixed into the insulative silicon compound layer, and the etching property and insulation property changes in accordance with the impurity concentration. As will be described hereinafter, sufficient insulation property and etching stop property are provided by limiting the impurity concentration to not more than 10at%, preferably not more than 5at%.

The investigations have been made as to changes of the etching property and electrical insulation property of a semiconductor device substrate with the impurity concentration in the insulative silicon compound layer ( $\text{SiO}_2$ ) resulting from diffusion of Zr and Y which are elements constituting the crystalline insulation layer (YSZ). The results are shown in Table 3.

Table3

Relation between Etching property and  
Electric insulation and  
Impurity concentration in SiO<sub>2</sub> Layer

5	-----								
	Zr, Y	1at%	3at%	5at%	7at%	10at%	12at%	15at%	20at%
	-----								
	Etch.	E	E	G	G	G	F	N	N
	-----								
10	Insl.	E	E	E	E	G	F	N	N
	-----								

The etching property has been checked after  
placed in HF 1% solution (20°C) for 10min. or longer.

As regards etching:

15 E: not etched.

G: partly etched on the surface

F: partly solved

N: solved

The electric insulation property has been  
20 checked on the basis of breakdwon when 10V is applied  
accross thickness 50nm.

As regards insulation:

E: property was particularly good

G: property was good

25 F: breakdwon was partly observed

N: breakdown occurred

As will be understood from Table 3, in the

case of such a semiconductor device substrate, the Zr  
Y which are structure elements of the YSZ are diffused  
into the  $\text{SiO}_2$  layer. The etching property and  
insulation property change with the concentration of  
5 the impurities (Zr+Y). If the concentration of the  
impurity (Zr+Y) is not more than 10at%, the insulation  
property is excellent for use as an insulation film,  
and if the concentration is not more than 7at%,  
particularly, not more than 5at%, the etching property  
10 is also excellent. In consideration of the results,  
according to the present invention, the component  
element of the material constituting the crystalline  
insulation layer 3 diffusing into the insulative  
silicon compound layer 2 is made of more than 10at%,  
15 preferably not more than 5at%.

The comparison with respect to the etching  
property and the electrical insulation property has  
been made between the oxide layer (insulative silicon  
compound layer) formed between the YSZ and the silicon  
20 substrate with introduction of non-active gas such as  
Ar or the like and the oxide layer (comparison  
example) formed between the YSZ and the silicon  
substrate with introduction of oxygen causing reaction  
with the metal. The results are shown in Tables 4 and  
25 5.

Table 4

Etching property

HF 1% solution (20°C)

-----				
5	time	1min.	5min.	10min.
-----				
	Present invention			
	SiO <sub>2</sub> (100nm)	E	E	E
-----				
10	Reactive			
	sputtering			
	SiO <sub>2</sub> (100nm)	G	F	N
-----				

15       The etching property has been checked after  
placed in HF 1% solution (20°C).

As regards etching:

E: not etched.

G: partly etched on the surface

F: partly solved

20       N: solved

Table 5  
Electric Insulation  
(1-20V)

5	Volt	1V	5V	10V	15V	20V
	Present invention					
	SiO <sub>2</sub> (100nm)	E	E	E	G	G
10	Reactive sputtering					
	SiO <sub>2</sub> (100nm)	F	FN	N	N	N

The electric insulation property has been checked on the basis of breakdown when 20V is applied across thickness 100nm.

As regards insulation:

E: property was particularly good

G: property was good

20 F: breakdown was partly observed

N: breakdown occurred

As will be understood from Tables 4 and 5, the oxide layer provided by the sputtering in the non-active gas atmosphere according to the present invention exhibits good etching property and electrical insulation property. On the contrary, the oxide layer provided by a reactive sputtering exhibits

poor insulation property and etching stop function,  
and it is not suitable for a semiconductor substrate  
or a substrate for micro machining. In the foregoing  
Embodiments, the substrate temperature is 600°C or  
5 800°C. However, it has been confirmed that same  
advantageous effects are provided when it is 400°C.  
In the foregoing embodiments, the crystal layer of YSZ  
is grown using a multiple oxide target comprising  $Y_2O_3$   
and  $ZrO_2$ , but it is possible to grow the crystal layer  
10 using a  $SrTiO_3$  as the target. By using  $Al_2O_3$  for the  
target, the crystal layer of  $Al_2O_3$  can be similarly  
grown, and similarly, a crystal layer of  $MgO$  or  $ZrO_2$   
can be grown.

While the invention has been described with  
15 reference to the structures disclosed herein, it is  
not confined to the details set forth and this  
application is intended to cover such modifications or  
changes as may come within the purpose of the  
improvements or the scope of the following claims.

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